UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,684	07/31/2003	Magdy Salama	2929-0223P	7661

7590 03/28/2005

Larry J. Palguta
Honeywee Law Department
3520 Westmoor Street
South Bend, IN 46628

EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,684	SALAMA ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 9 and 26 are objected to because of the following informalities: lines 3 and 2 respectively: "0-to28" [sic]. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 7-12, 18-22, and 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelly (US 4,251,857) in view of Gallios et al (US 4,893,227).

Claims 1 and 18; Shelly discloses a high-voltage power supply and method, comprising: a power scaling section (10) receiving an input voltage signal (Vin) and converting the input voltage signal to a controllable DC voltage (e.g. C1); a push-pull converter (Q2, Q3) for converting the controllable DC voltage to a high-frequency wave and wherein the generated high-voltage DC output is varied as the controllable DC voltage varies (abstract).

However, Shelly does not disclose a voltage multiplier receiving the high-frequency wave generated by the push-pull converter and performing successive voltage doubling operations to generate a high-voltage DC output.

Gallios et al teaches a two stage full-wave Cockroff-Walton high voltage multiplier 20 for receiving high frequency wave generated by a push pull converter for performing successive voltage doubling operations to generate a high voltage dc output in order to provide high output voltage to a load requiring very high output voltage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shelly to include a voltage multiplier for receiving high frequency wave generated by a push pull converter for performing successive voltage doubling operations to generate a high voltage dc output in order to provide high output voltage to a load requiring very high output voltage as taught by Gallios et al.

Claims 7 and 24; Gak et al further disclose the high-frequency wave is a square wave.

Claims 8, 25, 29 and 30; Gallios et al disclose wherein the frequency of said high-frequency wave is approximately 100 kHz (col. 5 line 31).

Claims 9 and 26; Gak et al further disclose the controllable DC voltage is in the range of approximately 0-to 28 kV.

Claims 10 and 27; Gak et al further disclose in the power supply generates an output voltage of in the range of approximately 0-to-30 kV, DC.

Claims 11 and 28; Gak et al further disclose in the high-frequency wave has an amplitude of approximately 0-to-1 kV.

Claim 12; Gak et al further disclose wherein the control module is an analog controller.

Claim 19; Shelly further disclose: controlling the scaling and converting steps in accordance with a command signal.

Claim 20; Shelly further disclose wherein the power scaling section includes a switching element, a duty cycle of which controls the amplitude of the controllable DC voltage, and the control module outputs a gate switching signal to the switching element of the power scaling section as a function of a desired output voltage of the high-voltage power supply.

Claim 21; Shelly further disclose wherein the control module receives a feedback signal based on the output of the power scaling section to adjust the gate switching signal.

Claim 22; Shelly further disclose wherein the push-pull converter includes a plurality of switching elements and a transformer for generating the high-frequency wave, and the control module outputs gate switching signals to the switching elements of the push-pull converter to control the frequency of the high-frequency wave.

5. Claims 2-6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelly (US 4,251,857) and Gallios et al (US 4,893,227) in view of Gak et al (US 6,141,225).

Claim 2; Shelly and Gallios et al disclose the claimed subject matter in regards to claim 1 supra, except for a control module for controlling both the power scaling section and the push pull converter.

Gak et al teach using one control module (19) for controlling the power scaling section and the push-pull converter.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize one controller to control both the power scaling section and the push pull converter as taught by Gak et al in place of two separate controllers in order to reduce manufacturing costs.

Claim 3; Gak et al further disclose wherein the power scaling section includes a switching element (12), a duty cycle of which controls the amplitude of the controllable DC voltage, and the control module outputs a gate switching signal (20) to the switching element (12) of the power scaling section (11) as a function of a desired output voltage of the high-voltage power supply.

Claim 4; Gak et al further disclose wherein the control module receives a feedback signal (16) based on the output of the power scaling section to adjust the gate switching signal (20).

Claim 5; Gak et al further disclose wherein the push-pull converter includes a plurality of switching elements (14A, 14B) and a transformer (15) for generating the high-frequency wave, and the control module outputs gate switching signals (CLK-PPA, CLK-PPB) to the switching elements (14A, 14B) of the push-pull converter (13) to control the frequency of the high-frequency wave.

Claims 6 and 23; Gak et al further disclose the switching elements are MOSFET switching elements.

6. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelly (US 4,251,857) in view of Gallios et al (US 4,893,227) and further in view of in view of Adasko et al (US 5,414,224).

Claims 13-17; Shelly and Gallios et al disclose the claimed subject matter in regards to claim 1 supra, except for the voltage multiplier includes voltage doubler stages on a circuit board and the high-voltage power supply further comprises an insulation system associated with the circuit board. And, the insulation system is a multi-layer system of n layers of insulation and m conducting strips positioned between successive insulating layers; wherein the insulation system is a field-controlled multi-layer insulation system. And lastly, the plurality of voltage doubler stages are divided among multiple circuit boards, separate from the power scaling section and the push-pull converter.

First, it has been held that forming in one piece an article which has formerly been formed in two pieces and put together (such as integrating circuit components on a circuit board) involves only routine skill in the art. *Howard v. Detroit Stove works*, 150 U.S. 164 (1893). Therefore, integrating parts on a circuit board is routinely obvious to one having ordinary skill in the art.

Secondly, duplication of parts is well known in the art; since it has bee held that mere duplication of the essential working parts of a device (such as connecting plural circuit boards together) involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Therefore, duplicating multiple voltage doubler circuit boards is routinely obvious to one having ordinary skill in the art.

Adasko et al teach forming a multilayered printed circuit board having layers with insulation between; and conducting strips between as well.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit combination of Shelly and Gallios et al to include

the voltage multiplier on a circuit board and further comprising an insulation system associated with the circuit board comprising insulating layers and conducting strips to form a field-controlled multi-layer insulation system in order to form an integrated small form multilayered printed circuit board for use in an electronic power supply circuit. And further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Shelly and Gallios et al to include plural circuit boards separate from separate from the power scaling section and the push-pull converter in order to provide a plurality of separate voltage circuits to provide high voltage power to a plurality of different loads, since duplicating parts is routine to those skilled in the art.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/21/05

Gary L. Laxton
Primary Examiner
Art Unit 2838